IN THE CLAIMS:

Please amend claims 1, and 3 as follows, and delete claims 5 and 6:

1. (Currently Amended) A hybrid tester architecture for testing ~~and repairing~~ a plurality of semiconductor devices in parallel, each semiconductor device having a predetermined number of pins, the hybrid tester architecture including:

a plurality of formatting circuits, each having data input circuitry and clock input circuitry, the plurality of formatting circuits adapted for a one-to-one correspondence with each pin of each semiconductor device;

shared timing circuits coupled to the clock input circuitry, each of the shared timing circuits operative to generate programmed timing signals and adapted for coupling to more than one pin of the semiconductor devices; and

a plurality of data circuits coupled to the data input circuitry, each data circuit of the plurality of data circuits adapted for a one-to-one correspondence with each pin of each semiconductor device and operative to generate drive data associated with each individual device pin.

2. (Previously Amended) A hybrid tester architecture according to claim 1 wherein:

the plurality of data circuits comprises a plurality of memory blocks, each memory block corresponding to one of the predetermined number of pins.

3. (Currently Amended) A hybrid tester architecture according to claim 1 and further including:

a capture memory for storing fail data relating to the plurality of semiconductor devices; and redundancy analyzer circuitry for processing the fail~~ure~~ data into a repair solution.

4. (Previously Amended) A hybrid tester architecture according to claim 3 and further including a computer workstation and wherein the redundancy analyzer is coupled to the computer workstation and operative, after generating repair solutions, to transmit the repair solutions to the computer workstation.

5. (Cancelled) A method of testing a plurality of semiconductor devices, each of the devices having a plurality of pins and redundant row and column addresses, the method including the steps:

generating test data signals unique to each of the plurality of pins;

clocking the test data signals through unique formatting circuitry with shared timing signals;

applying the test data signals to the plurality of semiconductor devices;

detecting and storing failure data relating to the plurality of semiconductor devices;

analyzing the failure data to generate repair solutions for each of the plurality of semiconductor devices.

6. (Cancelled) A hybrid tester architecture for testing and repairing a plurality of semiconductor devices in parallel, each semiconductor device having a predetermined number of pins, the hybrid tester architecture including:

means for generating test data unique to each of the plurality of pins;

means for clocking the unique test data through unique formatting circuitry with shared timing signals;

means for applying the test signals to the plurality of semiconductor devices;

means for detecting and storing failure data relating to the plurality of semiconductor devices; and

means for analyzing the failure data to generate repair solutions for activating certain of the redundant rows and columns for each of the plurality of semiconductor devices.